

MITSUBISHI MICROCOMPUTERS  
**M50752-PGYS**

**PIGGYBACK for M50752-XXXSP, M50757-XXXSP**

**DESCRIPTION**

The M50752-PGYS is an EPROM mounted-type micro-computer employing a silicon gate CMOS process and was designed for developing programs for single-chip, 8-bit microcomputers M50757-XXXSP/M50752-XXXSP. The M50752-PGYS, being housed in a piggyback-type 52-pin shrink DIP, is compatible with the M50752-XXXSP.

There is a 28-pin socket on the upper surface so that the M5L2732K or the M5L2764K EPROM may be used.

The M50752-PGYS simplifies the development of programs for the M50757-XXXSP/M50752-XXXSP and is excellent for making prototypes.

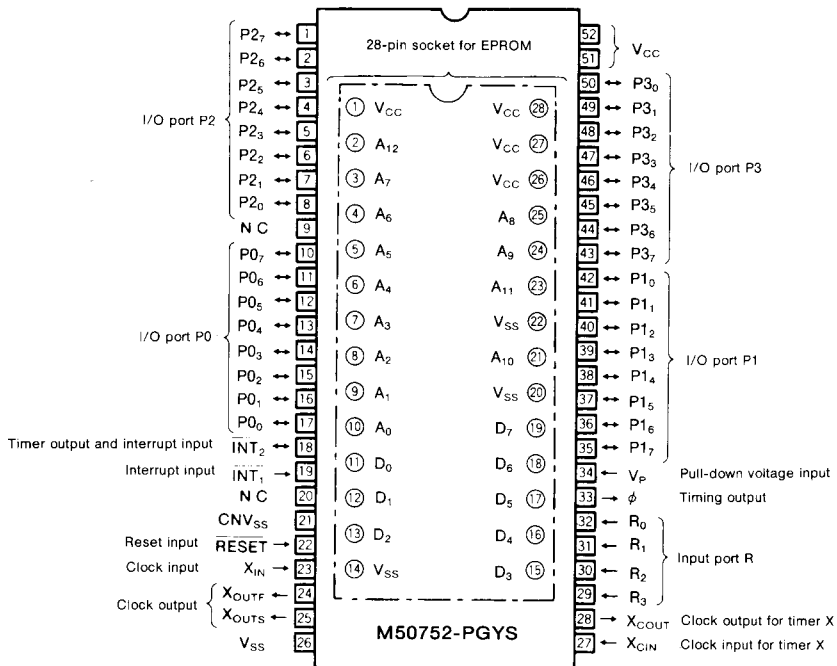
**DISTINCTIVE FEATURES**

- Differences with the M50752-XXXSP/M50757-XXXSP are:
  - (1) ROMless, EPROM is attached externally
  - (2) Suitable EPROM is the M5L2732K or the M5L2764K.

**APPLICATION**

Development of programs for VCR, tuners, and audio equipment.

**PIN CONFIGURATION (TOP VIEW)**



Outline 52S1M

The symbol "□" indicates socket for EPROM.  
 NC: No connection.

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**PIN DESCRIPTION**

| Pin                                | Name                           | Input/<br>Output | Functions   |
|------------------------------------|--------------------------------|------------------|---|
| V <sub>CC</sub><br>V <sub>SS</sub> | Supply voltage                 |                  | Power supply inputs 5V±10% to V <sub>CC</sub> , and 0V to V <sub>SS</sub> .   |
| CNV <sub>SS</sub>                  | CNV <sub>SS</sub>              |                  | This is usually connected to V <sub>SS</sub> .  |
| V <sub>P</sub>                     | Pull-down voltage              | Input            | This is the input voltage pin for the pull-down transistor of ports P1, P3, P2 <sub>6</sub> and P2 <sub>7</sub> .   |
| RESET                              | Reset input                    | Input            | To enter the reset state, the reset input pin must be kept at a "L" for more than 2μs (under normal V <sub>CC</sub> conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.   |
| X <sub>IN</sub>                    | Clock input                    | Input            | This chip has an internal clock generating circuit. To control generating frequency, a resistor is connected between the X <sub>IN</sub> and X <sub>OUTS</sub> or the X <sub>OUTF</sub> pins. If an external clock is used, the clock source should be connected to the X <sub>IN</sub> pin and the X <sub>OUTS</sub> and X <sub>OUTF</sub> pins should be left open. |
| X <sub>OUTS</sub>                  | Clock output                   | Output           | This is output pin from internal clock generating circuit. The generating frequency can be controlled by connecting a resistor between this pin and X <sub>IN</sub> pin.  |
| X <sub>OUTF</sub>                  | Clock output                   | Output           | This is output pin from internal clock generating circuit. The generating frequency can be controlled by connecting a resistor between this pin and X <sub>IN</sub> pin.  |
| φ                                  | Timing output                  | Output           | This is the timing output pin.  |
| X <sub>CIN</sub>                   | Clock I/O for timer X          | Input            | These are I/O pins of the clock oscillating circuit for the timer X. To control generating frequency, an external ceramic or a quartz crystal oscillator is connected between the X <sub>CIN</sub> pin and X <sub>COUT</sub> pin.   |
| X <sub>COUT</sub>                  |                                | Output           |   |
| INT <sub>1</sub>                   | Interrupt input                | Input            | This is the lowest order interrupt input pin.   |
| INT <sub>2</sub>                   | Time output or interrupt input | I/O              | This is in common with an output for the time X and an interrupt input pin.   |
| R <sub>0</sub> ~R <sub>3</sub>     | Input port R                   | Input            | Port R is a 4-bit input port.   |
| P0 <sub>0</sub> ~P0 <sub>7</sub>   | I/O port P0                    | I/O              | Port P0 is an 8-bit I/O port with directional registers allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is N-channel open drain.   |
| P1 <sub>0</sub> ~P1 <sub>7</sub>   | Output port P1                 | Output           | Port P1 is an 8-bit output port. The output structure is P-channel open drain.  |
| P2 <sub>0</sub> ~P2 <sub>7</sub>   | I/O port P2                    | I/O              | Port P2 is an 8-bit I/O port and has basically the same functions as port P0. For P2 <sub>6</sub> and P2 <sub>7</sub> pins, output structure is P-channel open drain, and a pull-down transistor is built in between the V <sub>P</sub> pin.  |
| P3 <sub>0</sub> ~P3 <sub>7</sub>   | Output port P3                 | Output           | Port P3 is an 8-bit output port and has basically the same functions as port P1.  |
| A <sub>0</sub> ~A <sub>12</sub>    | Output port A                  | Output           | Port A outputs the address of the EPROM loaded on the top side of the package.  |
| D <sub>0</sub> ~D <sub>7</sub>     | Input port D                   | Input            | Port D takes the input data from the EPROM loaded on the top side of the package.   |

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**EXPLANATION OF FUNCTION BLOCK OPERATION**

The differences between the M50752-PGYS and the M50757-XXXSP/M50752-XXXSP are explained below. As all other points are the same, only the differences are explained.

**MEMORY**

The memory map is shown in Figure 1. Instead of an internal ROM, an EPROM is mounted. The address of EPROM is 0100<sub>16</sub> to 1FFF<sub>16</sub>, having 7936 bytes. Other than this, the M50752-PGYS has the same functions as the M50752-XXXSP has. Actually, ROM area depends on EPROM capacity.

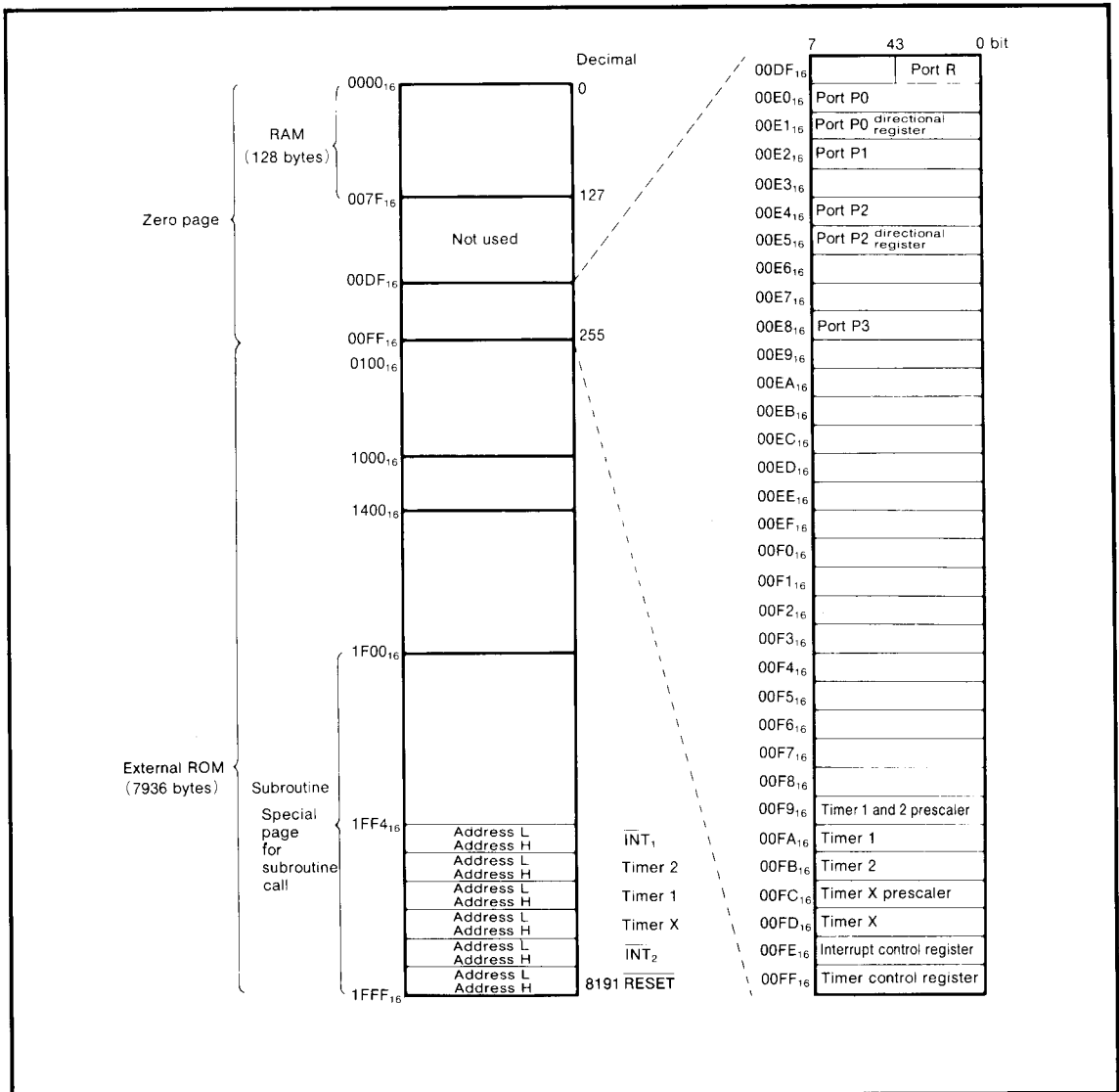


Fig.1 Memory map

**PIGGYBACK for M50752-XXXSP, M50757-XXXSP**

**PROCESSOR MODE**

External memory area differs from the M50757-XXXSP/M50752-XXXSP only in the memory expanding mode of the processor mode. Figure 2 shows the external memory area when the M50752-PGYS is in the memory expanding mode. All other processor modes are identical to those of the M50757-XXXSP/M50752-XXXSP.

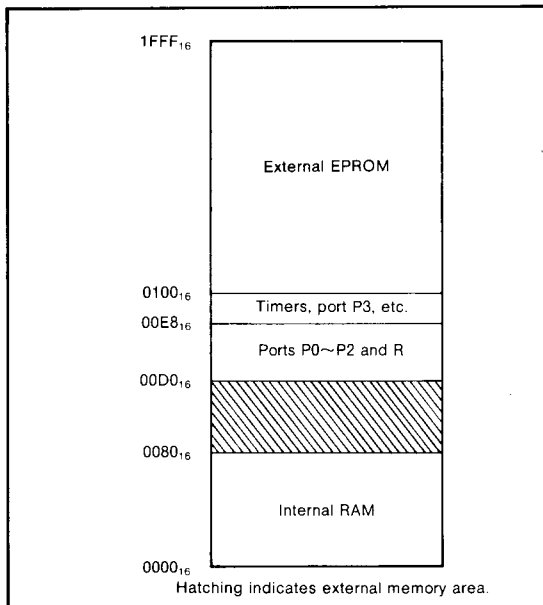


Fig.2 Memory map in memory expanding mode

**PRECAUTION FOR USE**

- (1) Because of the loading of the EPROM, the external dimensions differ from those of the M50757-XXXSP/M50752-XXXSP, being 19.0 × 50.8mm. Lower pin measurements are the same.
- (2) When developing programs with the M50752-PGYS, carefully consider the ROM capacity of the M50757-XXXSP/M50752-XXXSP.  
 In the case of the M50757-XXXSP, use the ROM area from 1400<sub>16</sub> to 1FFF<sub>16</sub>.  
 (In the case of the M5L2732K use the areas from 0400<sub>16</sub> to 0FFF<sub>16</sub>.)  
 In the case of the M50752-XXXSP, use the ROM area from 1000<sub>16</sub> to 1FFF<sub>16</sub>.  
 (In the case of the M5L2732K use the areas from 0000<sub>16</sub> to 0FFF<sub>16</sub>.)

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ABSOLUTE MAXIMUM RATINGS

| Symbol           | Parameter   | Conditions                                  | Ratings                                  | Unit |
|------------------|---|---|--|------|
| V <sub>CC</sub>  | Supply voltage  |   | -0.3~7                                   | V    |
| V <sub>P</sub>   | Supply voltage  |   | V <sub>CC</sub> -35~V <sub>CC</sub> +0.3 | V    |
| V <sub>I</sub>   | Input voltage R <sub>0</sub> ~R <sub>3</sub> , CNV <sub>SS</sub> , RESET, X <sub>IN</sub> , X <sub>CIN</sub> , D <sub>0</sub> ~D <sub>7</sub> | Measured using V <sub>SS</sub> as standard. | -0.3~7                                   | V    |
| V <sub>I</sub>   | Input voltage INT <sub>1</sub> , INT <sub>2</sub> , P <sub>0</sub> ~P <sub>07</sub> , P <sub>2</sub> ~P <sub>25</sub>                         |   | -0.3~13                                  | V    |
| V <sub>O</sub>   | Output voltage X <sub>OUTF</sub> , X <sub>OUTS</sub> , X <sub>COUT</sub> , φ, A <sub>0</sub> ~A <sub>12</sub>                                 | Output transistor is interrupted.           | -0.3~V <sub>CC</sub> +0.3                | V    |
| V <sub>O</sub>   | Output voltage INT <sub>2</sub> , P <sub>0</sub> ~P <sub>07</sub> , P <sub>2</sub> ~P <sub>25</sub>   |   | -0.3~13                                  | V    |
| V <sub>O</sub>   | Output voltage P <sub>1</sub> ~P <sub>17</sub> , P <sub>3</sub> ~P <sub>37</sub> , P <sub>6</sub> , P <sub>27</sub>                           |   | V <sub>CC</sub> -35~V <sub>CC</sub> +0.3 | V    |
| P <sub>d</sub>   | Power consumption   | T <sub>a</sub> =25°C                        | 1000                                     | mW   |
| T <sub>opr</sub> | Operating temperature   |   | -10~70                                   | °C   |
| T <sub>stg</sub> | Storage temperature   |   | -40~125                                  | °C   |

RECOMMENDED OPERATING CONDITIONS (T<sub>a</sub> = -10~70°C and V<sub>CC</sub>=5V±5% unless otherwise noted)

| Symbol                        | Parameter   | Limits              |      |                     | Unit |
|-------------------------------|---|---------------------|------|---------------------|------|
|                               |   | Min.                | Nom. | Max.                |      |
| V <sub>CC</sub>               | Supply voltage  | 4.75                | 5    | 5.25                | V    |
| V <sub>P</sub>                | Supply voltage  | V <sub>CC</sub> -33 |      | V <sub>CC</sub>     | V    |
| V <sub>SS</sub>               | Supply voltage  |                     | 0    |                     | V    |
| V <sub>IH</sub>               | "H" Input voltage R <sub>0</sub> ~R <sub>3</sub>  | 0.4V <sub>CC</sub>  |      | V <sub>CC</sub>     | V    |
| V <sub>IH</sub>               | "H" Input voltage RESET   | 0.8V <sub>CC</sub>  |      | V <sub>CC</sub>     | V    |
| V <sub>IH</sub>               | "H" Input voltage CNV <sub>SS</sub> , X <sub>IN</sub> , X <sub>CIN</sub>  | 0.8V <sub>CC</sub>  |      | V <sub>CC</sub>     | V    |
| V <sub>IH</sub>               | "H" Input voltage INT <sub>1</sub> , INT <sub>2</sub> , P <sub>0</sub> ~P <sub>07</sub> , P <sub>2</sub> ~P <sub>25</sub>                     | 0.8V <sub>CC</sub>  |      | V <sub>CC</sub>     | V    |
| V <sub>IH</sub>               | "H" Input voltage D <sub>0</sub> ~D <sub>7</sub>  | 0.45V <sub>CC</sub> |      | V <sub>CC</sub>     | V    |
| V <sub>IL</sub>               | "L" Input voltage R <sub>0</sub> ~R <sub>3</sub> , X <sub>IN</sub> , X <sub>CIN</sub>   | 0                   |      | 0.12V <sub>CC</sub> | V    |
| V <sub>IL</sub>               | "L" Input voltage RESET   | 0                   |      | 0.12V <sub>CC</sub> | V    |
| V <sub>IL</sub>               | "L" Input voltage CNV <sub>SS</sub> , INT <sub>1</sub> , INT <sub>2</sub> , P <sub>0</sub> ~P <sub>07</sub> , P <sub>2</sub> ~P <sub>25</sub> | 0                   |      | 0.2V <sub>CC</sub>  | V    |
| V <sub>IL</sub>               | "L" Input voltage D <sub>0</sub> ~D <sub>7</sub>  | 0                   |      | 0.15V <sub>CC</sub> | V    |
| f <sub>(X<sub>IN</sub>)</sub> | Internal clock oscillating frequency  |                     |      | 4                   | MHz  |

ELECTRICAL CHARACTERISTICS (V<sub>CC</sub> = 5V±5%, V<sub>SS</sub> = 0V, and f<sub>(X<sub>IN</sub>)</sub> = 4MHz unless otherwise noted)

| Symbol                             | Parameter  | Test conditions   | Limits |      |      | Unit |
|------------------------------------|--|---|--------|------|------|------|
|                                    |  |   | Min.   | Typ. | Max. |      |
| V <sub>OH</sub>                    | Output voltage P <sub>1</sub> ~P <sub>17</sub> , P <sub>3</sub> ~P <sub>37</sub> , P <sub>6</sub> , P <sub>27</sub>                                    | V <sub>CC</sub> =5V, T <sub>a</sub> =25°C<br>I <sub>OH</sub> =-12mA   | 3      |      |      | V    |
| V <sub>OH</sub>                    | Output voltage, φ, A <sub>0</sub> ~A <sub>12</sub>   | V <sub>CC</sub> =5V, T <sub>a</sub> =25°C<br>I <sub>OH</sub> =-2.5mA  | 3      |      |      | V    |
| V <sub>OL</sub>                    | Output voltage INT <sub>2</sub> , P <sub>0</sub> ~P <sub>07</sub> , P <sub>2</sub> ~P <sub>25</sub>  | V <sub>CC</sub> =5V, T <sub>a</sub> =25°C<br>I <sub>OL</sub> =10mA  |        |      | 2    | V    |
| V <sub>OL</sub>                    | Output voltage φ, A <sub>0</sub> ~A <sub>12</sub>  | V <sub>CC</sub> =5V, T <sub>a</sub> =25°C<br>I <sub>OL</sub> =5mA   |        |      | 2    | V    |
| V <sub>Tr+</sub> -V <sub>Tr-</sub> | Hysteresis INT <sub>1</sub> , INT <sub>2</sub>   | V <sub>CC</sub> =5V, T <sub>a</sub> =25°C   | 0.3    |      | 1    | V    |
| V <sub>Tr+</sub> -V <sub>Tr-</sub> | Hysteresis RESET   | V <sub>CC</sub> =5V, T <sub>a</sub> =25°C   |        | 0.4  | 0.7  | V    |
| I <sub>IL</sub>                    | Input leak current P <sub>0</sub> ~P <sub>3</sub> , CNV <sub>SS</sub> , RESET, X <sub>IN</sub> , X <sub>CIN</sub>                                      | V <sub>CC</sub> =5V, T <sub>a</sub> =25°C<br>0≤V <sub>I</sub> ≤5V   | -5     |      | 5    | μA   |
| I <sub>IL</sub>                    | Input current INT <sub>1</sub> , INT <sub>2</sub> , D <sub>0</sub> ~D <sub>7</sub> , P <sub>0</sub> ~P <sub>07</sub> , P <sub>2</sub> ~P <sub>25</sub> | V <sub>CC</sub> =5V, T <sub>a</sub> =25°C<br>0≤V <sub>I</sub> ≤5V   | -5     |      | 5    | μA   |
| I <sub>IL</sub>                    | Input leak current P <sub>1</sub> ~P <sub>17</sub> , P <sub>3</sub> ~P <sub>37</sub> , P <sub>6</sub> , P <sub>27</sub>                                | V <sub>CC</sub> =5V, T <sub>a</sub> =25°C<br>V <sub>CC</sub> -33V≤V <sub>I</sub> ≤V <sub>CC</sub>   | -33    |      | 33   | μA   |
| I <sub>CC</sub>                    | Supply current   | V <sub>CC</sub> =5V, T <sub>a</sub> =25°C<br>P <sub>2</sub> <sub>6</sub> and P <sub>27</sub> are V <sub>CC</sub> , output pins are left open<br>Input and I/O pins except P <sub>2</sub> <sub>6</sub> and P <sub>27</sub> are V <sub>SS</sub> |        | 3    | 6    | mA   |